REMARKS

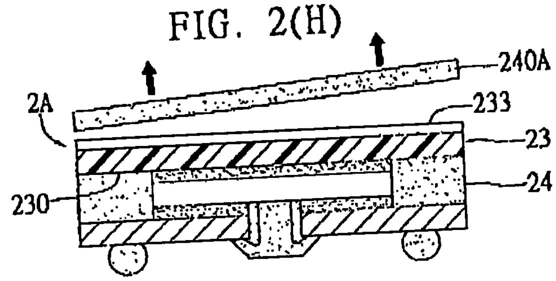
Claims 1-20 are pending in the application. Claims 1 and 12 have been amended by the present amendment.

In response to the objections to the drawings and specification, the specification has been amended on page 9 to clarify that "first surface 230" and "first layer 230" are the same. On page 6, last paragraph, the specification has been amended to insert a space between "chip" and "21". The grammar has also been corrected. No new matter has been added. It is respectfully requested that the specification and drawing objections be withdrawn.

Applicants claim a semiconductor package, including: a chip carrier; at least one chip mounted on the chip carrier; a heat sink having a first surface, a second surface opposing the first surface, and a plurality of side surfaces; <u>an interface layer formed on the second surface of the heat sink, where adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound</u>; and an encapsulant made of the molding compound for encapsulating the chip, and where the side surfaces of the heat sink are coplanar with side edges of the encapsulant.

Applicants' invention is exemplified by the following copy of FIG. 2(H).

FIG. 2(H)



As shown in FIG. 2(H), the heat sink 23 includes a first surface attached to the chip and an opposing second surface, the second surface having an interface layer 233 formed thereon, where adhesion between the interface layer 233 and a molding compound 240A is smaller than adhesion between the heat sink 23 and encapsulant 24.

The above-described semiconductor package can yield significant benefits. Because the molding compound does not readily adhere to the interface layer, after molding (as shown in FIG. 2(II)), the remaining molding compound 240A can be easily removed without requiring a subsequent deflash process and without damaging the bonding between the heat sink and the encapsulant (see page 9, first paragraph). Accordingly, resin flash can be prevented, and the heat-dissipating efficiency of the semiconductor package is assured. Moreover, by providing an interface layer, a plurality of heat sinks can be integrated as a heat sink module plate, mounted in a batch-type manner, and then singulated to form individual packages, because the interface layer of the Applicants' invention permits multiple packages to be formed without the problem of resin flash.

Claims 1-20 were rejected under 35 USC 112, second paragraph, as being indefinite because of the language "while adhesion between the interface layer and a molding compound being smaller than that between the first surface of the heat sink and the molding compound." Claims 1 and 12 have been amended to delete such language, and now clearly recite the interface layer as a separate element of the Applicants' claimed invention. It is respectfully requested that the rejection under 35 USC 112 be withdrawn.

Claims 1, 2, 4, 6, 9, and 10 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,288,900 to Johnson et al. (hereinafter "Johnson"). Claims 3 and 11 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,323,065 to Karnezos. Claim 5 was rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,127,724 to DiStefano. Claims 7 and 8 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,198,171 to Huang et al. Claims 12, 13, 15, 16, 19, and 20 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of U.S. Patent 6,236,568 to Lai et al. Claims 14 was rejected under 35 USC 103(a) as being unpatentable over Johnson in view of Lai et al., and further in view of Karnezos. Claims 17 and 18 were rejected under 35 USC 103(a) as being unpatentable over Johnson in view of Lai et al., and further in view of Huang et al. These rejections are respectfully traversed.

Johnson fails to teach or suggest a semiconductor package having an interface layer formed on a heat sink, where adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound. In FIGS. 15 and 16 of Johnson, as cited in the Office Action, a heat spreading cap 22 is formed by layers 40 and 41, which can be different materials having different combinations of CTE (see column 4, line 62 to column 5, line 9 and column 3, lines 23-25), but there is no teaching or suggestion for providing adhesion between one of these layers 40 or 41 and encapsulant 24 that is smaller than adhesion between the other layer 40 or 41 and the encapsulant 24. In Johnson, the heat spreading cap 22 is provided to reduce warpage or bending, but there is no disclosure of an interface layer which provides smaller adhesion between the interface layer and a molding compound as compared to between the heat sink and the molding compound.

None of the other cited references, either alone or in combination with Johnson, teach or suggest an interface layer formed on the second surface of the heat sink, wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

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Respectfully submitted,

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APPENDIX A: VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 6, last paragraph to page 7, line 7, the paragraph has been amended as follows:

The heat sink 23 has a first surface 230, a second surface 231 opposing the first surface 230, and a plurality of side faces 232 interconnecting the first surface 230 and the second surface 231. The second surface 231 is coated with a gold layer 233 thereon, while adhesion between the gold layer 233 and a molding resin used for forming the encapsulant 24 is smaller than that between the first surface 230 of the heat sink 23 and the molding resin. The first surface 230 is attached to the inactive surface 211 of the chip 21 through a thermally conductive adhesive 26, allowing heat generated by the [chip21] chip 21 to be directly transmitted to the heat sink 23 without passing through the encapsulant 24. Moreover, after the encapsulant is formed, the heat sink 23 merely has the first surface 230 thereof bonded to the encapsulant 24, while the side faces 232 and the gold layer 233 coated on the second surface 231 of the heat sink 23 are exposed to the outside of the encapsulant 24. That is, the encapsulant 24 fills a gap between the first surface 230 of the heat sink 23 and the upper surface 200 of the substrate 20. Additionally, while the heat sink 23 has the same surface area as the substrate 20, the exposed surface area of the heat sink 23 can be maximized so as to effectively improve the heat-dissipating efficiency.

On page 9, first paragraph, the paragraph has been amended as follows:

Referring finally to FIG. 2(H), the singulated semi-fabricated package 2A is heated for the [remained] remaining molding resin 240A on the gold layer 233 to be delaminated from the gold layer 233, due to the difference in thermal expansion coefficient between the molding resin used for forming the encapsulant 24 and the gold layer 233. It is required for the heating to be controlled in the condition of no delamination occurring between the first [layer] surface 230 of the heat sink 23 and the encapsulant 24. This allows the [remained] remaining molding resin [240 A] 240A to be easily removed from the gold layer 233 without damaging the bonding of the heat sink 23 to the encapsulant 24. Further, since the [remained] remaining molding resin 240A

can be completely removed from the gold layer 233, a subsequent deflash process is not necessary, which not only reduces the molding cost but also assures quality of the fabricated semiconductor package 2 (as shown in FIG. 1).

IN THE CLAIMS

Claims 1 and 12 have been amended as follows:

1. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

a heat sink having a first surface, a second surface opposing the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface <u>of the heat sink</u> is attached to the chip for interposing the chip between the chip carrier and the heat sink[, and the second surface is formed with an interface layer thereon, while adhesion between the interface layer and a molding compound being smaller than that between the first surface of the heat sink and the molding compound];

<u>an interface layer formed on the second surface of the heat sink, wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound;</u> and

an encapsulant made of the molding compound for encapsulating the chip and filling a gap between the first surface of the heat sink and the chip carrier, [while] <u>wherein</u> the interface layer and the side surfaces of the heat sink [being] <u>are</u> exposed to outside of the encapsulant, and the side surfaces of the heat sink [being] <u>are</u> in a coplane with side edges of the encapsulant.

12. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip;

a heat sink having a first surface, a second surface opposing the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the buffer pad for interposing the buffer pad between the heat sink and the chip so as to space the first surface from the chip[, and the second surface is formed with an interface layer thereon, while adhesion between the interface layer and a molding compound being smaller than that between the first surface of the heat sink and the molding compound];

an interface layer formed on the second surface of the heat sink, wherein adhesion between the interface layer and a molding compound is smaller than adhesion between the heat sink and the molding compound; and

an encapsulant made of the molding compound for encapsulating the chip and the buffer pad, and for filling a gap between the first surface of the heat sink and the chip carrier, [while] wherein the interface layer and the side surfaces of the heat sink [being] are exposed to outside of the encapsulant, and the side surfaces of the heat sink [being] are in a coplane with side edges of the encapsulant.